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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,264	01/29/2002	Koji Tomioka	NEC01P260-HYa	4190

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EXAMINER	
MARTIN, CIARA A	

ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,264	TOMIOKA, KOJI	
	Examiner	Art Unit	
	Ciara Martin	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment filed on May 12, 2006. Claims 1-20 are pending. Claims 1-4, 6-7, 9 and 11-17 were amended. Claims 18-20 were added new. Claims 1-20 represent a computer system, CPU and memory installed apparatuses, and input/output control apparatuses.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Houssein et al. US 6,418,479 B1.

As per claim 1, Houssein teaches a clustered computer system comprising:

a plurality of CPU and memory installed apparatuses having at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3); and

a plurality of input/output control apparatuses (2:66-3:13, claim 5, Fig. 3),

wherein said CPU and memory installed apparatuses and said input/output control apparatuses are connected to each other by a network (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 2, Houssein teaches a computer system comprising:

a plurality of CPU and memory installed apparatuses having at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3);

a plurality of input/output control apparatuses (2:66-3:13, claim 5, Fig. 3), and

a network connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other (2:22-37, 3:14-25, claim 5, Fig. 3),

wherein each of said CPU and memory installed apparatuses comprises communication means for transmitting an input/output instruction issued by at least one CPU of said plurality of CPU and memory installed apparatuses to at least one of said input/output control apparatuses assigned in advance to said at least one CPU and memory installed apparatuses via said network, and receives a response from at lease one of said input/output control apparatuses via said network (2:22-37, 3:14-25, claim 5, Fig. 3), and

wherein each of said input/output control apparatuses comprises communication means for receiving an input/output instruction from at least one CPU and memory installed apparatuses assigned in advance to at least one of said plurality of input/output control apparatuses via said network, and transmits a response to said input/output instruction to said at least one CPU and memory installed apparatuses via said network (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 3, Houssein teaches a computer system according to claim 2, wherein said communication means of each of said input/output control apparatuses comprises:

means for receiving the input/output instruction as being effective only when the source of the input/output instruction received via said network is a CPU and memory installed apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 4, Houssein teaches a computer system according to claim 2, wherein said communication means of each of said CPU and memory installed apparatuses comprises:

means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 5, Houssein teaches a computer system according to claim 2, wherein said network is also used for communications between said plurality of CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 6, Houssein teaches a computer system according to claim 3, wherein said communication means of each of said CPU and memory installed apparatuses comprises:

means for receiving a response as being effective only when the source of the response received via said network is an input/output control apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 7, Houssein teaches a computer system according to claim 5, wherein said communication means of each of said CPU and memory installed apparatuses comprises:

means for communicating with other CPU and memory installed apparatuses via said network.

As per claim 8, Houssein teaches a computer system according to claim 7, wherein the communications between said plurality of CPU and memory installed apparatuses are communications for accessing memories installed on other CPU and memory installed apparatuses.

As per claim 9, Houssein teaches a computer system according to claim 2, further comprising:

means for, when either one of said CPU and memory installed apparatuses fails to operate due to a fault, assigning said input/output control apparatuses which has been used by a faulty CPU and memory installed apparatuses to another normal CPU and memory installed apparatuses hereby to continue system operation (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 10, Houssein teaches a computer system according to claim 9, wherein an active one of the CPU and memory installed apparatuses which is using another input/output control apparatuses is used as said other normal CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 11, Houssein teaches a computer system according to claim 9, further comprising a backup CPU and memory installed apparatuses, said backup CPU and memory installed apparatuses being used as said other normal CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 12, Houssein teaches a computer system according to claim 2, further comprising:

at least one backup input/output control apparatuses, and means for, when either active one of said input/output control apparatuses fails to operate due to a fault, assigning said backup input/output control apparatuses to said CPU and memory installed apparatuses which has been using the faulty input/output control apparatuses thereby to continue system operation (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 13, Houssein teaches a computer system comprising:

a CPU and memory installed apparatuses having at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3);

an input/output control apparatuses (2:66-3:13, claim 5, Fig. 3); and

a communication cable connecting said CPU and memory installed apparatuses and said input/output control apparatuses to each other (2:22-37, 3:14-25, claim 5, Fig. 3),

wherein said CPU and memory installed apparatuses having communication means for transmitting an input/output instruction issued by said CPU to said input/output control apparatuses via said communication cable, and receives a response from said input/output control apparatuses via said communication cable (2:22-37, 3:14-25, claim 5, Fig. 3), and

wherein said input/output control apparatuses comprising communication means for receiving an input/output instruction from said CPU and memory installed apparatuses via said communication cable, and transmits a response to said

input/output instruction to said CPU and memory installed apparatuses via said communication cable (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 14, Houssein teaches a CPU and memory installed apparatuses comprising:

at least one CPU and at least one memory (2:22-37, 2:49-65, claim 5, Fig. 3);

communication means for communicating with an external circuit comprising an input/output control apparatus, transmitting an input/output instruction issued by said CPU to said input/output control apparatuses which has been assigned in advance, and receiving a response from said input/output control apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3); and

a single board on which said CPU, said memory, and said communication means are mounted (2:66-3:13, claim 5, Fig. 3).

As per claim 15, Houssein teaches a CPU and memory installed apparatuses according to claim 14, wherein said communication means comprises:

means for receiving said response as being effective only when the source of the received response is the input/output control apparatuses which has been assigned in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 16, Houssein teaches an input/output control apparatuses comprising:

an input/output control circuit for controlling a peripheral device based on an input/output instruction (2:66-3:13, claim 5, Fig. 3); and

communication means for communicating with an external circuit comprising a CPU and memory installed apparatus, for receiving an input/output instruction from said CPU and memory installed apparatuses which has been set in advance and transferring said input/output instruction to said input/output control circuit, and for transmitting a response to said input/output instruction to said CPU and memory installed apparatuses (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 17, Houssein teaches an input/output control apparatuses according to claim 16, wherein said communication means comprises:

means for receiving said input/output instruction as being effective only when the source of the received input/output instruction is the CPU and memory installed apparatuses which has been set in advance (2:22-37, 3:14-25, claim 5, Fig. 3).

As per claim 18, Houssein teaches a computer system according to claim 2, wherein each of said plurality of input/output control apparatus further comprises and input/output (I/O) device (2:66-3:13, claim 5, Fig. 3).

As per claim 19, Houssein teaches a computer system according to claim 18, wherein said input/output (I/O) device is connected to a peripheral device (Fig. 3).

As per claim 20, Houssein teaches a computer system according to claim 18, wherein said input/output (I/O) device is connected to a second network (Fig. 3).

Response to Arguments

3. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ciara Martin whose telephone number is 571-272-7507. The examiner can normally be reached on M-F 6:30- 4:00 with second Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on 571-272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CM
7/17/06

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